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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,941	07/29/2003	Roger A. Fratti	12-19	9094

7590 07/16/2004

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EXAMINER	
MAGEE, THOMAS J	
ART UNIT	*PAPER NUMBER*
2811	

DATE MAILED: 07/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/628,941	FRATTI ET AL.	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *April 26, 2004* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections – 35 U.S.C. 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 – 8, and 13 - 16 are rejected as being unpatentable over Hebert (US 6,091,110) in view of Zommer (US 6,162,665), Sherman ("Chemical Vapor Deposition for Microelectronics," Noyes Publ., Westwood, N.J. (1987), p.68), Sergey Savastiouk et al. ("Atmospheric Downstream Plasma," European Semiconductor (June, 1998), pp. 1 – 4)

3. Regarding Claim 1, Hebert discloses a method for controlling the curvature (and stress) (Col.1, lines 54 – 59) of a device (Col. 2, lines 35 – 39), wherein a thin stress compensation layer (24) (Figure 1C) (Col. 2, line 54), is formed on a substrate over the surface of the device. Hebert does not disclose that the deposited oxide film has a tensile stress. However, Sherman discloses (p. 68, 2nd para.) that the stress in the oxide film is tensile, wherein the tensile stress in the oxide film provides "stress relief" in the device (Col. 1, lines 54 – 59). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Sherman with Hebert to obtain a film having tensile stress to relieve residual stress within the device.

Additionally, Hebert does not disclose thinning of the substrate. Zommer discloses (Col. 2, lines 8 – 12) that the breakdown voltage is altered by changing the thickness of the substrate to alter resistivity by aggressive backsurface grinding, polishing, or thinning (Col.2, lines 40 – 43). Such techniques, however, are notoriously well known to introduce damage that will alter the residual stress (Savastiouk et al., p. 1, para. 4, 6, 7). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the procedures of Zommer in Hebert to obtain a backsurface thinned substrate with altered resistivity and breakdown voltage.

4. Regarding Claims 2 and 14, Hebert discloses that the stress compensation layer comprises a thin film (24) (Figure 1C).

5. Regarding Claim 3, Hebert discloses that the power transistor comprises a DMOS device (Col. 2, lines 35 – 36).

6. Regarding Claim 4, Hebert does not disclose that the substrate is thinned by aggressive backside removal procedures. Zommer discloses that the removal is done by backsurface grinding, polishing or thinning. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the procedures of Zommer in Hebert to obtain a backsurface "thinned" substrate for improved device properties.

7. Regarding Claims 5 and 6, Hebert discloses that a CVD silicon oxide layer is deposited

(Col. 2, lines 54 – 56).

8. Regarding Claim 7, Hebert does not disclose a procedure for obtaining a "desired" curvature. It would have been obvious to one of ordinary skill in the art at the time of the invention to obtain a "desired" curvature by performing a series of tests to optimize the curvature, wherein parametric thinning and deposition of an oxide would be used as variables. It has been ruled by the court that *"where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."*

9. Regarding Claims 8 and 15, Hebert discloses that the thin film serves as an encapulant (Col. 1, lines 54 – 57).

10. Regarding Claims 13 and 16, Hebert discloses a power transistor device (Col. 2, lines 35 – 39), wherein a thin film (24) (Figure 1C), comprising a CVD silicon oxide (Col. 2, line 54), is formed on a substrate as a stress compensation layer. Hebert does not disclose that the deposited oxide stress compensation layer has a tensile stress. However, Sherman discloses (p. 68, 2nd para.) that the stress in the oxide film is tensile, wherein the tensile stress in the oxide film provides "stress relief" in the device (Col. 1, lines 54 – 59). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Sherman with Hebert to obtain a film having tensile stress to relieve residual stress within the device.

Additionally, Hebert does not disclose thinning of the substrate. Zommer discloses (Col. 2, lines 8 – 12) that the breakdown voltage is altered by changing the thickness of the substrate to alter resistivity by aggressive backsurface grinding, polishing, or thinning (Col.2, lines 40 – 43). Such techniques, however, are notoriously well known to introduce damage that will alter the residual stress (Savastiouk et al., p. 1, para. 4, 6, 7). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the procedures of Zommer in Hebert to obtain a backsurface thinned substrate with altered resistivity and breakdown voltage.

Finally, although Hebert does not explicitly disclose that the device is part of an integrated circuit, it is inherent that the fabrication procedures and intended utilization are part of an integrated circuit manufacturing methodology, wherein the power transistor is incorporated with other elements to produce a working system.

11. Claims 9 – 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hebert in view of Sherman, Zommer, and Savastiouk et al., as applied to Claims 1 – 8, and 13 – 16, and further in view of Wilson et al. ("Handbook of Multilevel Metallization for Integrated Circuits, Noyes Publ., Westwood, New Jersey, (1993) pp. 223 – 225).

12. Regarding Claims 9 and 10, Hebert does not disclose that the application of the stress compensating layer either maintains or alters the curvature of the device. Wilson et al. dis-

close that the stress in the structure will cause the wafer to bend (p.223, 2nd para.) and thus alter the curvature according to Equation 13. Hence, the radius of curvature will be inversely proportional to the residual stress and the film thickness, such that, for a given stress, the radius of curvature will either change or remain the same with the application of films of varying thickness. As discussed for Claim 7, optimization can be used to determine the values for thinning and film thickness to either maintain curvature or change curvature. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wilson et al. with Hebert to obtain values of the curvature for determining the effectiveness of stress relief.

13. Regarding Claims 11 and 12, Hebert does not disclose a method for monitoring the curvature of the device. Wilson et al. disclose (pp. 223 – 224) that an optical laser system can be utilized to measure curvature using an off-axis technique. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wilson et al. with Hebert to obtain the radius of curvature for power transistor devices.

Response to Arguments

14. Although some of the arguments are moot in terms of the new grounds of rejection, a few comments can be made regarding others. Applicant's contention that residual stress is not present in back thinned substrates is not correct. Back thinning has been used in the art for over 35 years and the existence of such stress is notoriously well known, as discussed in the Office Action. There is more than adequate rationale for combining Hebert and

Zommer, since it is shown that back thinning will produce positive benefits in Hebert. Further, since the stress relief in Hebert is related to the presence of a film with a tensile stress (Sherman), the back thinned substrates containing residual stress through the substrate ((Savastiouk) can be "relaxed" using the invention of Hebert.

Conclusions

7. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee,** whose telephone number is **(703) 305 5396.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee,** can be reached on **(703) 308-1690.** The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306.**

ORI NADAV
patent examiner

Thomas Magee